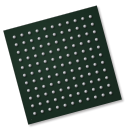
OV580

ASIC product brief

Stand Alone ISP Bridge Chip for High Definition 3D Applications



OMNIVISION's OV580 is an image signal processor (ISP) bridge chip for high definition (HD) 3D applications. The OV580 includes a built-in-advanced ISP for high-quality image and video streaming. It accepts two video inputs from MIPI camera serial interfaces and supports up to 1080p HD at 30 frames per second (fps) or 1280 x 800 pixels operating at 60 fps for dual streaming 3D applications in both RAW and YUV format.

Additionally, dual 2-lane MIPI input interfaces can be combined to form a single 4-lane MIPI input to convert a large resolution MIPI sensor to USB 3.0 output.

Find out more at www.ovt.com.

OMNIVISION®

OV580

Ordering Information

- **OV00580-B21G-1C** (lead-free)
  121-pin BGA

Applications

- HD 3D imaging applications

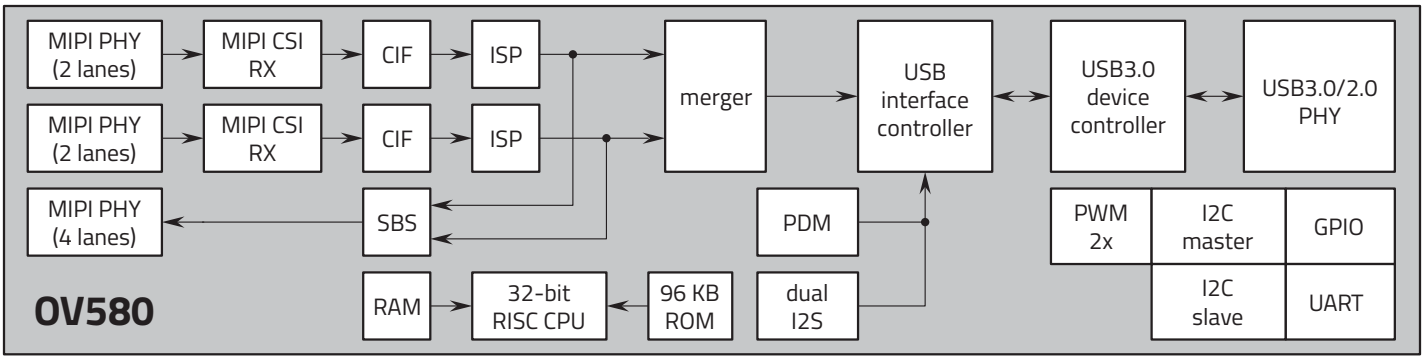
Technical Specifications

- **power supply:**
  - core: 1.2V ±10%
  - I/O: 3.3V / 2.5V / 1.8V ±10%
  - analog: 1.8V ±10% (MIPI) / 3.3V ±10% (USB)
- **power requirements:**
  - active: 460 mW
  - standby: 1.7 mA
- **temperature range:**
  - operating: -30°C to +70°C ambient temperature
- **package dimensions:** 8 x 8 x 1.2 mm

Product Features

- supports a maximum 3MP sensor input or EIS 1080p (maximum input width is 2208 pixels and maximum input height is 1536 lines) for ISP process
- supports dual 2-lane MIPI RX interface with maximum data transfer rate of 800 Mbps (MIPI RX 2x2 lane can combine dual 2-lane to single 4-lane MIPI RX to receive higher resolution sensor input, such as 8MP, 13MP sensors)
- supports RAW8, RAW10, RAW12 and YUV422 format input
- supports video class and audio class based on USB 3.0 interface
- built-in advanced image signal processor (ISP) for high quality images and video streaming, which features include:
  - AWB
  - AEC/AGC
  - AFC
  - DNS
  - gamma
  - special digital effects (SDE)
- supports two sets of external I2S audio input interface
- supports one MIPI TX 4-lane interface
- supports 3D mode processed images of up to 1920 x 1080 @ 30 fps or 1280 x 800 @ 60 fps
- embedded 32-bit RISC processor with 96 KB program memory
- on-chip PLL with an input clock frequency of 20 MHz
- embedded 1.2V regulator, that supports a typical 240 mA current and maximum 480 mA current
- supports 1K bits of one time programmable memory (OTP)
- supports two sets of SCCB master and one set of SCCB slave
- core 1.2 power can be supplied by external power supply or internal regulator

Functional Block Diagram



Version 1.3, August 2024

4275 Burton Drive
Santa Clara, CA 95054
USA

Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com

OMNIVISION®