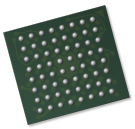
OV680



ASIC product brief

Four-Channel Stand-Alone MIPI Bridge Controller for High Definition Multi-Camera Applications

OMNIVISION's OV680 companion chip is a multi-sensor bridge solution that combines images from four sensors into a single data stream. Ideally suited for high definition (HD) multi-camera applications, the OV680 has four 1-lane MIPI receivers for four video inputs or two 2-lane MIPI for two video inputs, a 2-lane MIPI transmitter for video output, and a built-in 8-bit microcontroller.

The OV680 features integrated image signal processors (ISPs), allowing it to process one, two, or four video streams simultaneously. The companion chip can output 2x 720p video at 60 frames per second (fps), or 4x VGA video at 120 fps.

Find out more at www.ovt.com.

OMNIVISION®

OV680

Ordering Information

- **OV00680-B64G** (lead-free)
  64-pin BGA

Applications

- high definition multi-camera applications

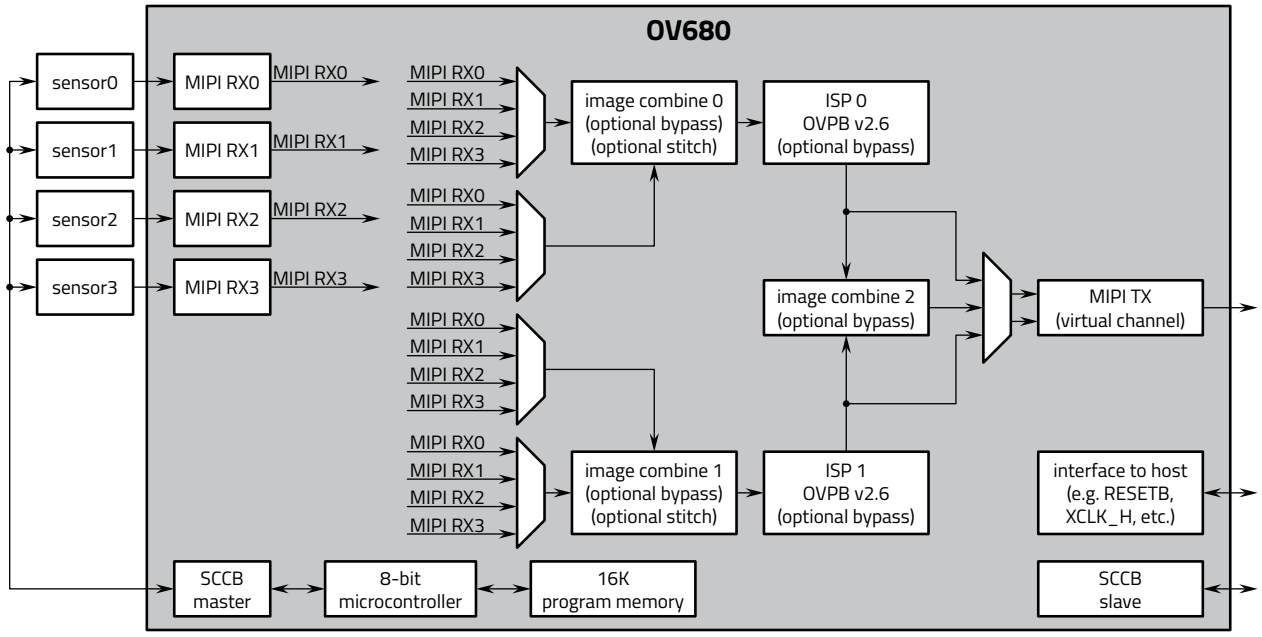
Technical Specifications

- **maximum image transfer rate:** 120 fps
- **power supply:**
  - core: 1.2V
  - analog: 2.8V
  - I/O: 1.8V
- **power requirements:**
  - hardware standby: 75 µW
- **temperature range:**
  - operating: -30°C to +70°C junction temperature
- **output formats:**
  - 8-bit and 10-bit RAW RGB data
  - YUV422 data
- **input clock frequency:** 6 ~ 27 MHz
- **package dimensions:** 5000 µm x 4500 µm

Product Features

- interfaces:
  - four one-lane MIPI receivers for video input
  - can combine to dual 2-lane video inputs
  - one channel two-lane MIPI transmitter for video output
  - up to 400 kHz SCCB with 13 MHz ~ 26 MHz input clock
  - three general purpose IO (GPIO)
  - one open drain output CMD_RDY
- on-chip PLLs:
  - system PLL - input clock frequency ranges from 13 MHz to 26 MHz
  - MIPI speed - 5x or 10x of system clock for RAW, 4x or 8x of system clock for YUV
- image signal processor (ISP)
  - AEC/AGC/AWB
  - two ISPs, one for each input video stream
  - max resolution: 1280 x 800
  - max frame rate: 60 fps at 720p, 120 fps at VGA, 240 fps at QVGA
  - defect pixel correction (DPC)
  - lens shading correction (LENC)
- SCCB:
  - one SCCB master to control sensors
  - one SCCB slave to take the commands from host controller
  - 7-bit SCCB slave device ID is fixed to 0x35 (0x6A for write, and 0x6B for read)
  - supports SCCB clock 100 kHz and 400 kHz
- data format:
  - input: RAW
  - output: RAW 8/10-bit, YUV422
- microcontroller:
  - 8-bit microcontroller running at the system clock
  - 16 KByte program memory
- power supply:
  - 1.8V for DOVDD, 2.8V for MIPI and PLL analog
  - internal regulator generates 1.2V DVDD from DOVDD for the digital core circuit
  - hardware standby mode: initiated by pulling PWDN high, whole system halts and input clock is gated
  - software standby mode: initiated by register, whole system except the SCCB slave block halt

Functional Block Diagram



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